DEC STD 176-4 Surface Mount Printed-Wiring Board Acceptance Criteria

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ABSTRACT: This standard specifies end product criteria for surface mount rigid printed-wiring boards (PWBs) that have been fabricated by or purchased for Digital Equipment Corporation.

APPLICABILITY: It is mandatory that, whether fabricated in Digital manufacturing facilities or purchased from qualified suppliers, all PWBs meet or exceed all applicable specifications defined in this standard, unless modified by applicable Digital engineering drawings and specifications.

STATUS: APPROVED 11-Nov-1992; use VTX SMC for current status.

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1 INTRODUCTION

This standard specifies end product criteria for rigid surface mount technology (SMT) printed-wiring boards (PWBs) that have been fabricated or purchased by Digital Equipment Corporation.

1.1 SCOPE

This standard specifies the final end product acceptance criteria for rigid surface mount printed-wiring boards of the types specified in *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*, in this document, and the product's design data base. This standard does not apply to flex circuits or ceramic printed-wiring substrates.

1.2 RESPONSIBILITIES

This section describes specific responsibilities of persons or organizations for fulfilling the requirements of this standard.

1.2.1 Digital Organizations

All internal organizations involved in the fabrication, procurement, and use of PWBs are responsible for understanding and complying to the requirements in this document and for providing information to keep the document up-to-date.

1.2.2 Suppliers

Suppliers under contract to produce surface mount PWBs for Digital must comply with the requirements of this standard.

1.2.3 PWB Standards Committee

Refer to the applicable section of EL-SM176-00 *Printed-Wiring Board Manual*, for a list of committee members. This committee is chaired by Gerald G. Gagnon.

2 GENERAL REQUIREMENTS

Whether fabricated in Digital manufacturing facilities or purchased from qualified suppliers, all surface mount PWBs shall meet or exceed all applicable specifications defined in this standard, to be modified only by related Digital drawings and specifications.

2.1 TERMINOLOGY

The definitions of all conventional nonsurface mount printed-wiring terms used in this standard shall be as specified in *DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*.

2.2 COMPOSITION AND PROCESSING

The composition and processing of the types of PWBs covered by this standard shall be as described in DEC STD 016-0.

2.3 OVERALL CONFIGURATION AND CONSTRUCTION

The conductive and nonconductive patterns, including fingers and plated-through holes (PTHs), and the overall configuration of each board, including slots, notches, and cutouts, shall be as specified in the product data base and master drawing and/or other documentation extracted from the product data base.

2.4 MICROSECTIONING AND MAGNIFICATION

Microsection inspections shall be in accordance with the latest revision of IPC-TM-650, *Test Methods Manual*.

The appropriate minimum magnification is specified in Table 1. Higher magnification may be used to verify conformance to this standard's visual and functional requirements. Defects found at higher magnification are considered defects.

Table 1: Magnification

Item(s) Inspected	Minimum Magnification (X)
Overall cosmetic quality	Visual inspection
Board features	2
Referee inspection of board features	10
Plating quality in microsections	200
Plating and soldermask thickness in microsections	400
Solder microstructural features	Scanning electron microscopy – 1000

2.5 ROUNDING CONVENTION

See DEC STD 176-0, subhead 2.5.

2.6 FABRICATION MATERIALS

Fabrication materials such as copper-clad laminates, prepreg, copper foil, soldermask, and plating materials are specified in DEC STD 176-0.

2.7 WORKMANSHIP AND CLEANLINESS

There shall be no contaminants or imperfections that affect form, fit, function, reliability, serviceability, or processability within a module assembly application.

Ionic (electrical) contaminants shall not exceed the amounts specified in DEC STD 176-0, subhead 2.7.

2.8 IDENTIFICATION MARKINGS

Digital and supplier PWB identification markings are specified in DEC STD 176-0.

2.9 COLORS

All PWBs shall be fabricated in the colors normally produced by processing the fabrication materials specified in the text under subhead 2.6. Discolorations caused by approved processing are acceptable; discolored terminal areas that will be soldered are acceptable provided that they satisfy the solderability requirements specified in the text under subhead 7.4.

Regardless of the colors used and the degree of discoloration, the manufacturer's name or trademark and the Digital part identifier (part number and revision) must be legible.

2.10 DIMENSIONS AND TOLERANCES

All dimensions and tolerances specified in this standard are applicable only to finished boards, as supplied by the board manufacturer, and are expressed in inches and millimeters.

3 OUTSIDE CONFIGURATION

Tolerances or limits for length, width, thickness, warpage, slots, notches, cutouts, straightness, parallelism, and squareness are specified in the following sections.

3.1 DIMENSIONS

Length and width tolerances and thickness limits are as specified in DEC STD 176-0.

3.2 WARPAGE

Warpage (bow or twist) shall be measured in accordance with the procedure defined in DEC STD 176-0, Appendix C. The maximum warpage (bow or twist) shall be as listed in Table 2.

Table 2: Maximum Warpage, SMT and Mixed-Mount Technology Boards

Nominal Board Thickness		Maximum Warpage Ratio
in	mm	inch/inch
$\leq$ 0.089	$\leq$ 2.26	0.007
$\geq$ 0.090 through 0.250	$\geq$ 2.29 through 6.35	0.005

3.3 SLOTS, NOTCHES, AND CUTOUTS

Unless otherwise specified, the dimensional tolerances for slots, notches, and cutouts shall be as specified in DEC STD 176-0.

3.4 STRAIGHTNESS, PARALLELISM, AND SQUARENESS

For board edges, the straightness, parallelism, and squareness shall be as specified in DEC STD 176-0.

4 BASE MATERIAL VISUAL CHARACTERISTICS

Acceptable and unacceptable surface conditions, chips, cracks, fibers, haloing, delamination, crazing, and measling are specified in DEC STD 176-0.

5 HOLES

The criteria for nonplated and plated holes are specified in the following subheads.

5.1 NONPLATED DRILLED AND PUNCHED HOLES

Unless otherwise specified, requirements for nonplated hole diameters, hole pattern accuracy, chips, cracks, fibers, haloing, delamination, and missing/extra holes are specified in DEC STD 176-0.

5.2 PLATED-THROUGH HOLES

The criteria for PTH diameters, plating thicknesses, and other characteristics for PTHs are specified in the following sections.

5.2.1 Plated Hole Diameters

Unless otherwise specified, PTH diameter tolerances for conventional component holes, tooling holes, and 0.038 inch (0.95 mm) nominal via holes shall be according to DEC STD 176-0, Table 8. The preferred method of measurement is with pin gauges.

5.2.2 Plating Thicknesses/Composition

All plating thicknesses and characteristics shall be evaluated according to DEC STD 176-0.

For surface mount PWBs with less than or equal to 10 layers and a nominal thickness less than 0.090 inch (2.28 mm), the thickness of copper on the walls of all PTHs shall be according to DEC STD 176-0, regardless of the base material.

For surface mount PWBs that have a base material with glass transition temperature (Tg) greater than or equal to 200°C, all PTH copper thicknesses shall be according to DEC STD 176-0, regardless of layer count and board thickness.

For surface mount PWBs with greater than or equal to 10 layers and a nominal thickness greater than or equal to 0.090 inch (2.28 mm), the thickness of copper on the wall of all PTHs shall be an absolute minimum of 0.001 inch (0.25 mm) when base materials with Tg less than 200°C are used.

NOTE

Tg is determined using thermomechanical analysis (TMA).

Fused tin-lead and solder shall have a minimum thickness of 0.000150 inch (0.00381 mm) at crest. Total coverage of the entire surface mount device pad surface with free tin-lead (no exposed copper or copper-tin intermetallics) is required. Total coverage of surface mount device pad side wall preferred but not required. The composition of fused tin-lead or solder shall be 50-70% tin (30-50% lead).

5.2.3 Other PTH Characteristics

Unless otherwise specified, other PTH characteristics such as plating nodules, plating voids, resin smear, metallic plating/foil cracks, circumferential copper separation from base material, and others as defined in DEC STD 176-0, shall be determined using microsectioning and appropriate magnification (refer to text under subhead 2.4). The criteria for these PTH characteristics shall be as specified in DEC STD 176-0.

6 CONDUCTORS AND PADS

Conductor widths and spacing, pad diameters, registration, plating thicknesses, edge characteristics, and other characteristics are specified in the following sections.

6.1 CONDUCTOR WIDTHS

As inspected and measured for edge definition in accordance with the text under subhead 2.2.3 of IPC-TM-650, *Test Methods Manual*, the minimum conductor widths shall be as specified in DEC STD 176-0.

6.1.1 Thermal Impedance Conductors (Legs)

The minimum total width of thermal relief conductors on power/ground planes shall be as specified in DEC STD 176-0.

6.2 SPACING

For all conductors and pads, minimum conductor-to-conductor, conductor-to-pad, and pad-to-pad spacing (including SMT pads) shall be as specified in DEC STD 176-0.

6.3 PAD DIAMETERS

This section describes requirements for pad diameters.

6.3.1 Intrusive Through-Hole Mounted Components

Minimum outer-layer and inner-layer pad diameters for component and via holes shall be as specified in DEC STD 176-0.

6.3.2 Surface Mount Devices

There are additional requirements for surface mount device pads. Surface mount device pads are rectangular pads with rounded ends that surface mount devices are placed onto and soldered. The surface mount device pads are arranged in specific configurations known as footprints, which are unique to each surface mount device. Refer to the footprint examples in Figure 1.

The nominal surface mount device footprint pad sizes and tolerances for the various SMT features as measured at the pad surface (top of ETCH) are as follows:

SMT pad geometry (length or width)		Tolerance	
in	mm	in	mm
> 0.020	> 0.51	± 0.0030	± 0.0076
≤ 0.020	≤ 0.51	± 0.0015	± 0.0038

On an Acceptable Quality Level (AQL) basis, it is acceptable to assess finished surface mount device pad sizes for product acceptance based on measuring the finest pitch surface mount device pads present.

6.3.3 Fiducials

In addition to surface mount device pads, SMT PWB technology introduces two new types of surface pads: fiducial pads and test pads.

Fiducial pads are circular surface pads (without holes) that serve as reference targets for automated surface mount device onsertion and assembly. All SMT PWBs will have circuit level fiducials placed in all four corners of the PWB in specific locations that are defined in the product data.

For additional component placement accuracy, any SMT PWB containing 0.050 inch (1.27 mm) pitch surface mount devices with lead counts greater than or equal to 44 pins, as well as all SMT PWBs with 0.025 inch (0.64 mm) pitch surface mount devices, will have component level fiducial pads.

Component level fiducial pads will appear within the surface mount device footprint pattern in diagonally opposite locations. The precise locations are defined in the product data. Refer to Figure 1.

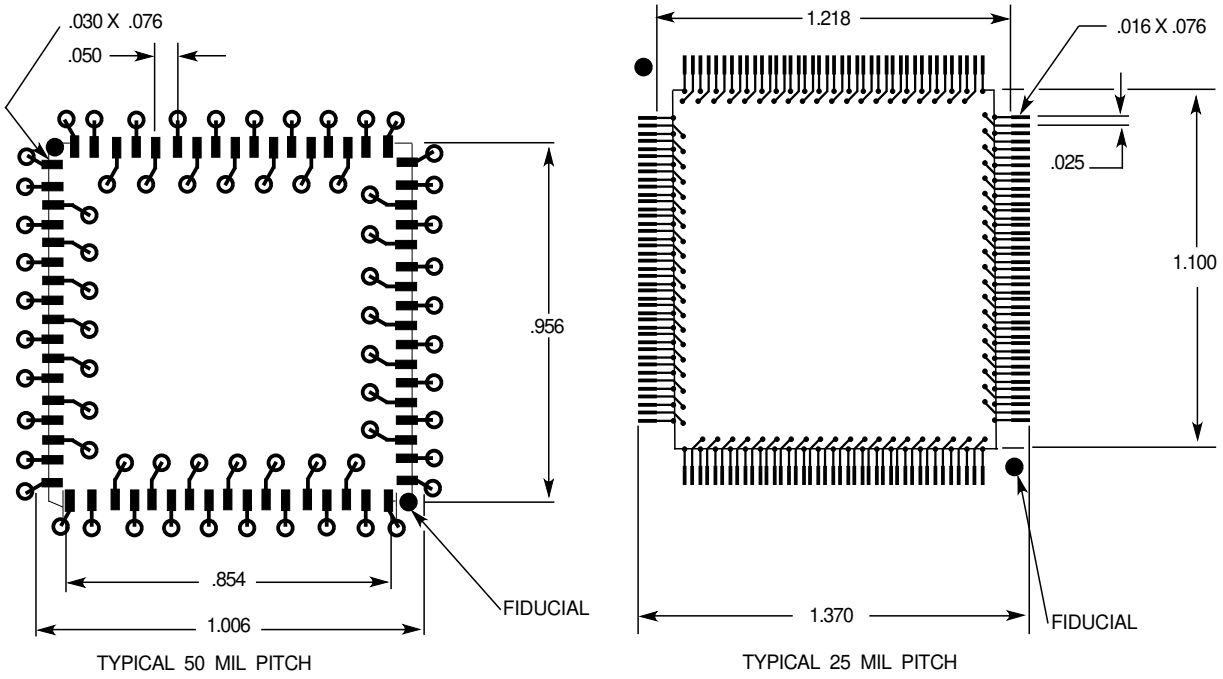
Circuit or component level fiducials are typically 0.040 inch (±1.0 mm) nominal diameter ±0.005 inch (0.127 mm).

Note: All dimensions shown in Figure 1 are in inches.

6.3.4 Test Pads

SMT test pads are selected and assigned in all SMT designs for assembly test access after the SMT PWB has been assembled. Specific locations of SMT test pads are defined in the product data. SMT test pads are typically round and may or may not contain a plated-through hole. Typical diameters as defined in the product's design data base are 0.035 inch (0.889 mm) and 0.040 inch (1.0 mm). SMT test pad size tolerance is ±0.003 inch (±0.076 mm).

Figure 1: Examples of Typical Surface Mount Device Footprint Patterns



6.4 REGISTRATION

This section describes requirements for registration.

6.4.1 Outer-Layer Features

Unless otherwise specified, the preferred registration and maximum allowable outer-layer misregistration for conventional component PTH pads and holes for SMT PWBs shall be as specified in DEC STD 176-0.

PWB location accuracy from computer assisted design (CAD) shall be determined using a coordinate measuring machine with an accuracy of ± 0.0002 in (0.0005 mm).

In addition, there are special registration requirements for SMT PWBs based on the following SMT features.

For 0.050 inch (1.27 mm) pitch surface mount device pads:

a. Surface mount device pad-to-pad registration within each footprint pattern must be within 0.0042 inch (0.1066 mm) True Position Diameter.

b. Surface mount device pad-to-fiducial registration within each footprint pattern must be within 0.0042 inch (0.1066 mm) True Position Diameter.

For fine pitch (0.025 (0.635 mm) or less) surface mount device pads:

a. For PWBs with a maximum distance between fine pitch SMT footprints of 16.5 in (419 mm) or less, all device pads shall be located within a 0.0080 in (0.203 mm) diameter true position.

   This requirement only applies to that area of the board that contains fine pitch SMT parts.

The registration of an 0.040 inch (1.0 mm) diameter test via/pad to 0.157 inch (3.98 mm) tooling holes identified as TH1 and TH2 in the product data or mechanical drawing shall be within 0.033 inch (0.84 mm) True Position Diameter.

The registration of an 0.035 inch (0.89 mm) diameter test via/pad to 0.157 inch (3.98 mm) tooling holes identified as TH1 and TH2 in the product data or mechanical drawing shall be within 0.020 inch (0.51 mm) True Position Diameter.

6.4.2 Inner-Layer Features

Unless otherwise specified, the preferred registration and maximum allowable inner-layer misregistration for conventional component PTH pads and holes for all SMT PWBs shall be as specified in DEC STD 176-0.

6.4.2.1 Power/Ground Planes and Thermal Impedance Areas

Unless specified otherwise, the preferred registration and maximum allowable inner-layer misregistration for conventional clearance (and thermal impedance) pads and holes for all SMT PWBs are as specified in DEC STD 176-0.

6.5 PLATING THICKNESSES

As determined via microsectioning and appropriate magnification, according to text under subhead 2.4, the minimum conductor, component pad, via pad, and SMT test pad plating thicknesses shall be as defined in DEC STD 176-0, unless otherwise specified.

Unless otherwise specified, SMT fiducial pads are not subject to any minimum thickness requirements as long as fiducial pad size and location tolerance requirements are met.

Surface mount device pad thicknesses and coverage are critical for solderability and shall be microsectioned and evaluated independently from plated-through hole microsections. The criteria for SMT plating thickness are defined in Table 4 and Figure 2.

Table 3: SMT Plating Thicknesses

Plating Material	Minimum Thickness
Electroless copper	Sufficient for subsequent copper electroplating.
Electrolytic copper	0.001 inch (0.025 mm).
Fused tin-lead and solder	0.00015 inch (0.00381 mm) at crest. Total coverage of the entire surface mount device pad surface with free tin-lead (no exposed copper or copper-tin intermetallics). Total coverage of surface mount device pad side wall preferred but not required.

6.6 ETCH CHARACTERISTICS

As determined via microsectioning and appropriate magnification, according to text under subhead 2.4, etch characteristics shall be as defined in DEC STD 176-0, unless otherwise specified.

6.7 OTHER ETCH CHARACTERISTICS

Other SMT conductor and pad characteristics include blisters, breaks, delaminations, inclusions, nodules, nicks, scratches, pits, dents, and voids. Some of these visual imperfections in conductors, component pads, via pads, SMT test pads, and SMT fiducial pads are permitted within the maximum limits defined in DEC STD 176-0, unless otherwise specified. For SMT designs specifying SMOBC, also refer to *DEC STD 176-3 Printed-Wiring Board Acceptance Criteria for SMOBC (Soldermask Over Bare Copper) Product*.

Surface mount device pads have different requirements due to the critical effects that the defects noted above may impart to surface mount device solderability and solder joint reliability. Some visual imperfections are permitted within the following maximum limits.

a. Blisters, breaks, delaminations (lifting or peeling), pinholes, voids, inclusions, exposed copper, and surface nodules are not acceptable under any circumstances.

b. Minor surface nicks, scratches, pits, dents, and test probe marks are acceptable under the following circumstances.

   1. There is no exposed copper or copper-tin intermetallics on the surface, and minimum tin-lead thickness at crest, as well as tin-lead coverage over the

entire surface mount device pad surface, is maintained (no exposed copper-tin intermetallics).

2. For isolated pits, and dents, the maximum length in any direction does not exceed 0.010 inch (0.25 mm).
3. Surface mount device solderability is not affected.

c. Surface mount device pad edge nicks, nodules, and projections are acceptable if they do not cause the affected surface mount device pads to exceed the minimum spacing or pad size requirements.

7 PLATING CHARACTERISTICS

The following describes the required criteria related to Plating characteristics.

7.1 TIN-LEAD PLATING (FUSED)

Fused tin-lead characteristics for conductors, power/ground planes, component pads, via pads, and SMT test pads shall be as defined in DEC STD 176-0, unless otherwise specified.

For SMT designs specifying soldermask over bare copper finish, the solder coating thicknesses and other characteristics shall be as defined in DEC STD 176-3, unless otherwise specified.

When viewed with scanning electron microscopy (refer to text under subhead 2.4), fused tin-lead plating or solder coating on surface mount device pad surfaces shall not exhibit any evidence of burned plating, porous plating, surface films, or entrapped contaminants.

When viewed with scanning electron microscopy (refer to text under subhead 2.4), fused tin-lead plating or solder coating on surface mount device pad surfaces shall exhibit metallurgical microstructural features clearly outlining the boundaries between tin and lead phases consistent with the composition specified in the text under subhead 5.2.2. Refer to Appendix A for an illustration of acceptable microstructural features.

Fiducials and test pads are not solderable surfaces and as such may be exempted from minimum tin-lead (or solder) thickness/alloy requirements and may exhibit dewetting.

7.2 ADHESION

Adhesion of all plating shall be as defined in DEC STD 176-0, unless otherwise specified.

7.3 BOND STRENGTH (TERMINAL PULL STRENGTH)

Bond strength of PTHs shall be as defined in DEC STD 176-0, unless otherwise specified. Laminated blind vias are not subject to this requirement.

7.4 SOLDERABILITY

Solderability tests shall be in accordance with IPC-S-804, *Solderability Test Methods for Printed-Wiring Boards*. Regardless of the test method used, the following shall occur.

a. Surface mount device pads shall exhibit 100% wetting. Dewetting or pinholing is not allowed.

b. At least 95% wetting with 5% unconcentrated dewetting and pinholing allowed for PTH pads, PTH hole walls, and surface terminal (solderable) areas.

c. All nonterminal (nonsolderable) areas of surface power/ground planes and large etch widths not covered by soldermask may be dewetted.

d. Blistering, delamination (lifted conductors), or other forms of degradation of the conductive pattern are not allowed.

7.5 THERMAL STRESS (PTHs)

Thermal stress testing and requirements shall be as defined in DEC STD 176-0, unless otherwise specified.

8 FINGERS

Criteria for plating thickness, surface finish, porosity, unused fingers, adhesion, length, width, spacing, beveling, edge taper, and other characteristics shall be as defined in DEC STD 176-0, unless otherwise specified.

9 SOLDERMASK

Soldermask shall meet all requirements defined in DEC STD 176-0, unless otherwise specified. SMT exceptions are specified in the following subheads.

9.1 TYPES

A full soldermask, as described in DEC STD 016-0, shall cover both outside surfaces of all SMT PWBs. Any qualified and approved soldermask may be used for SMT products where via tenting is not required. For SMT designs where via tenting is required, dry film soldermask is recommended. The use of 0.004 in (0.101 mm) nominal dry film raw stock is not permitted on SMT products.

9.2 PLACEMENT

Soldermask is required for both sides of all SMT PWBs, unless otherwise specified.

9.2.1 Spacing/Coverage Requirements

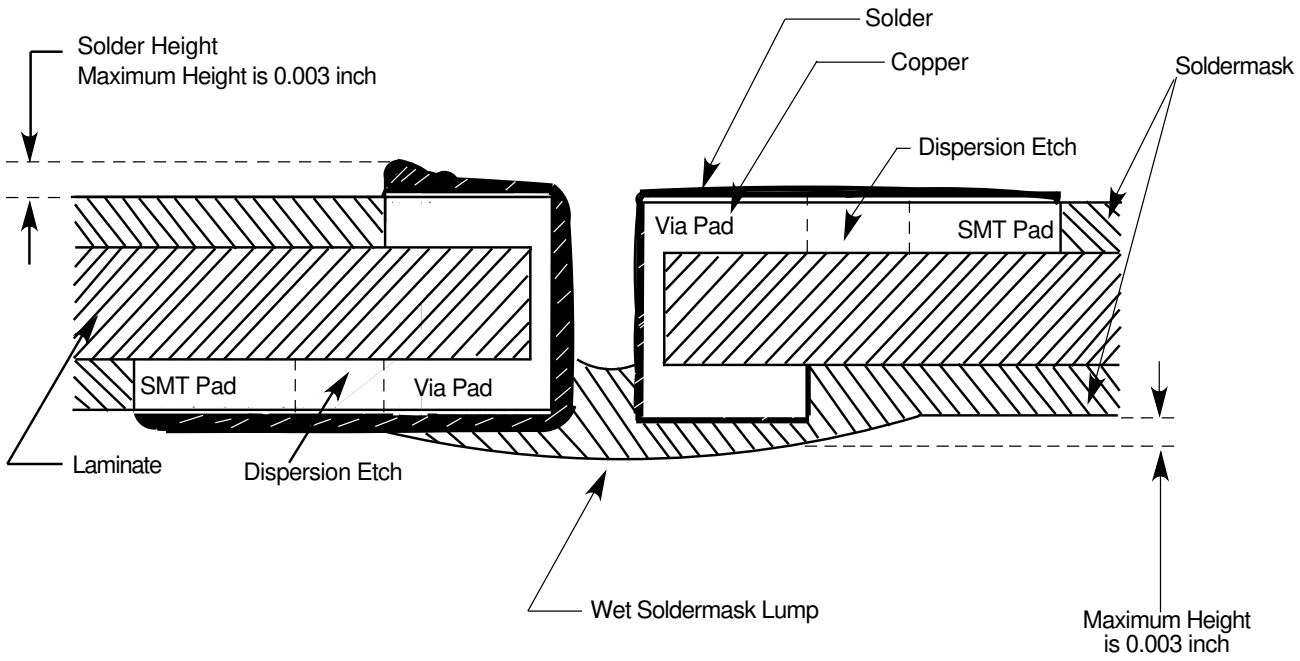
Soldermask spacing requirements shall be as defined in DEC STD 176-0, unless specified otherwise. SMT exceptions are as follows.

a. Exposed adjacent surface mount footprint pads designed with less than 0.015 inch (0.38 mm) pad-to-pad spacing are acceptable.

b. Under visual inspection, soldermask is not allowed on the surface of any surface mount device pads, SMT test pads, or fiducial pads.

c. There shall be no soldermask lumps or vertical solder protrusions extending greater than 0.003 inch (0.076 mm) beyond the normal height of the surrounding soldermask plane. Refer to Figure 3. In addition, all repairs must be performed in accordance with the requirements stated in *DEC STD 176-1 Printed-Wiring Board Repair Criteria,* subhead 5.5.1, list item b.

Figure 2: Maximum Height of Solder and Soldermask



9.3 CURE

Soldermask cure shall be as defined in DEC STD 176-0, unless otherwise specified.

9.4 SOLVENT AND FLUX RESISTANCE

Soldermask solvent and flux resistance shall be as defined in DEC STD 176-0, unless otherwise specified.

9.5 FLAMMABILITY

Soldermask flammability shall be as defined in *DEC STD 176-2 Printed-Wiring Board Product Safety Criteria*.

9.6 ABRASION RESISTANCE

Soldermask abrasion resistance shall be as defined in DEC STD 176-0, unless otherwise specified.

9.7 ADHESION

Soldermask adhesion shall be as defined in DEC STD 176-0, unless otherwise specified.

9.8 SOLDER RESISTANCE

For solder resistance, refer to DEC STD 176-0. In addition, the soldermask shall not exhibit any degradation after being submitted to the following processes.

Two cycles of vapor phase reflow at 215°C (419°F) for 90 seconds
One wave solder cycle at 254°C (491°F) for 5 seconds
Three repair cycles utilizing localized solder flow process at 254°C (491°F) for 15 seconds

9.9 OTHER SOLDERMASK CHARACTERISTICS

Other soldermask characteristics include blistering, voids, exposed conductors, and placement defects shall be as defined in DEC STD 176-0, unless otherwise specified.

10 MULTILAYER AND MULTISIGNAL-LAYER BOARDS

All applicable multisignal-layer PWB requirements shall be as defined in DEC STD 176-0, unless otherwise specified.

11 AUTOTHIEVING

Autothieving is a process that adds current density sinks (nonfunctional plating areas) to a printed-circuit board during imaging. When autothieving is used, it shall meet the requirements of DEC STD 176-0, unless otherwise specified.

12 BACKPANEL BOARDS

For backpanel PWBs, refer to DEC STD 176-0.

13 ELECTRICAL CHARACTERISTICS

Dielectric withstanding voltage (HIPOT), interconnection resistance, impedance, capacitance, continuity, and additional multilayer requirements shall be as defined in DEC STD 176-0, unless otherwise specified.

13.1 CONTINUITY

There shall be no opens or shorts in each conductor or group of interconnected conductors. Continuity for all SMT PWBs shall be electrically verified to 100% of all network endpoints (including surface mount device pads), or verified by equivalent means (for example, automated optical inspection).

14 ALLOWABLE REPAIRS

Digital personnel and personnel of suppliers not of Digital may perform repairs as defined in DEC STD 176-1. After repair, the board must meet all physical, electrical, cosmetic, workmanship, and cleanliness requirements specified in this standard.

15 PRODUCT SAFETY

The UL requirements for PWBs made by Digital are specified in DEC STD 176-2.

16 NONCONFORMING BOARDS

All nonconforming PWBs shall be processed in accordance with A-SP-7665075-00-0, *Procedure for Processing Nonconforming Material and In-Process Waiver*.

17 PACKAGING

In addition to good commercial practice in packaging, marking, shipping, and storing, PWB packaging requirements shall be as defined in DEC STD 176-0, unless otherwise specified.

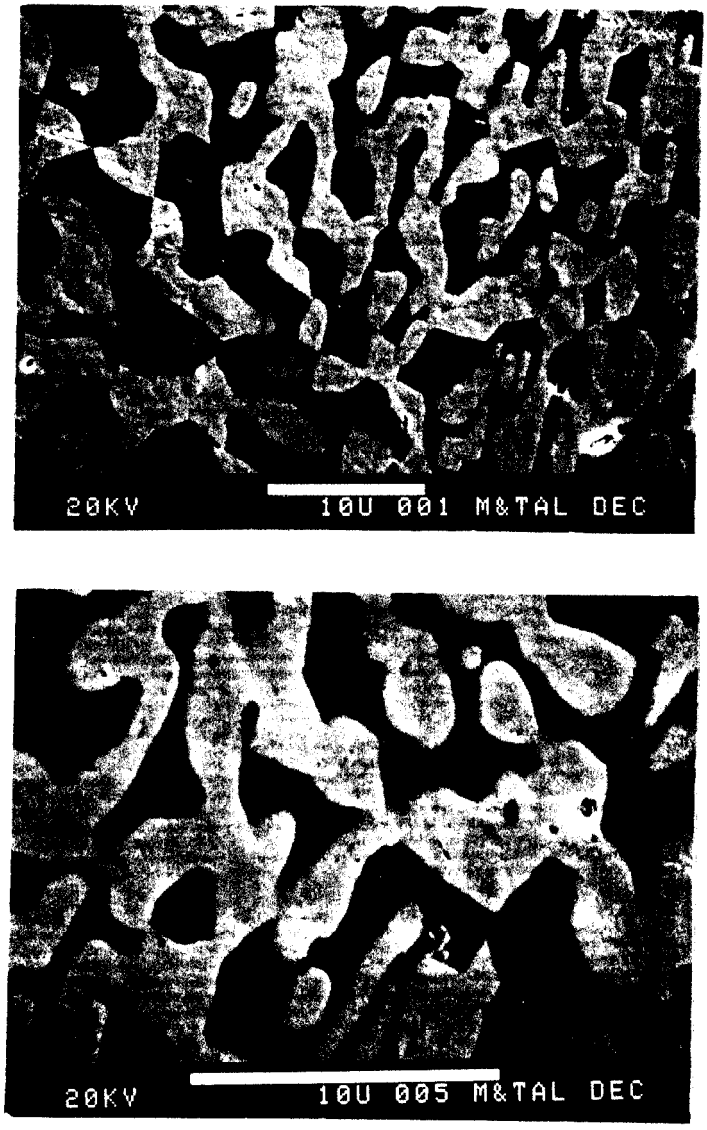
18 QUALITY ASSURANCE TESTS

Unless otherwise defined, all applicable quality assurance tests shall be as specified in DEC STD 176-0.

APPENDIX A ACCEPTABLE MICROSTRUCTURAL FEATURES

SMT pad surface microstructural features should be characteristic of eutectic (63/37), or near-eutectic, tin/lead solder compositions. The features should include a two-phase mixture of a lead-rich phase (white) and a tin-rich phase (gray) consistent with this composition range of solders. The surface should exhibit a generally clean condition, with minimal porosity or surface contaminant evident within the microstructural features.

Figure A–1: Acceptable Microstructural Features



APPENDIX B REFERENCED DOCUMENTS

B.1 Digital Documents, EL-Class

Document Number	Document Title
76-65075-00	*Procedure for Processing Non-Conforming Material and In-Process Waiver*
EL-00016-00	*DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*
EL-00176-01	*DEC STD 176-1 Printed-Wiring Board Repair Criteria*
EL-00176-02	*DEC STD 176-2 Printed-Wiring Board Product Safety Criteria*
EL-00176-03	*DEC STD 176-3 Printed-Wiring Board Acceptance Criteria for SMOBC (Soldermask Over Bare Copper) Product*
EL-SM176-00	*Printed-Wiring Board Manual*

B.2 Documents External to Digital

Document Number	Document Title
IPC-S-804	*Solderability Test Methods for Printed-Wiring Boards*
IPC-TM-650	*Test Methods Manual*

B.3 Ordering Information

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

Following are the sources for documents not available from Standards and Methods Control.

- Copies of IPC publications may be purchased from:
  Institute for Interconnecting and Packaging Electronic Circuits,
  7380 North Lincoln Ave., Lincolnwood IL 60646
  Telephone (708) 677-2850

APPENDIX C RELATED DOCUMENTS

C.1 Digital Documents, EL-Class

Document Number	Document Title
EL-MF299-00	*Printed-Circuit Boards/Modules: Cleaning Process Contamination*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

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